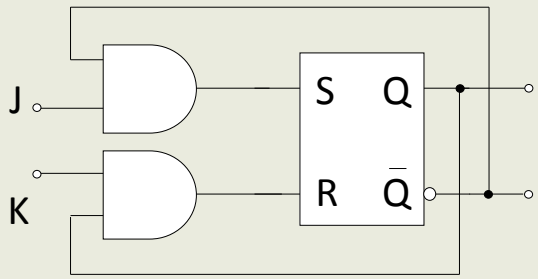
ЦИФРОВА СХЕМОТЕХНИКА

ЛЕКЦИЯ #7

Асинхронни JK тригери от RS тригер /ляво/ и директна структура /дясно/



$$Q^{t+1}_{SR} = S \vee \overline{R}Q^t$$

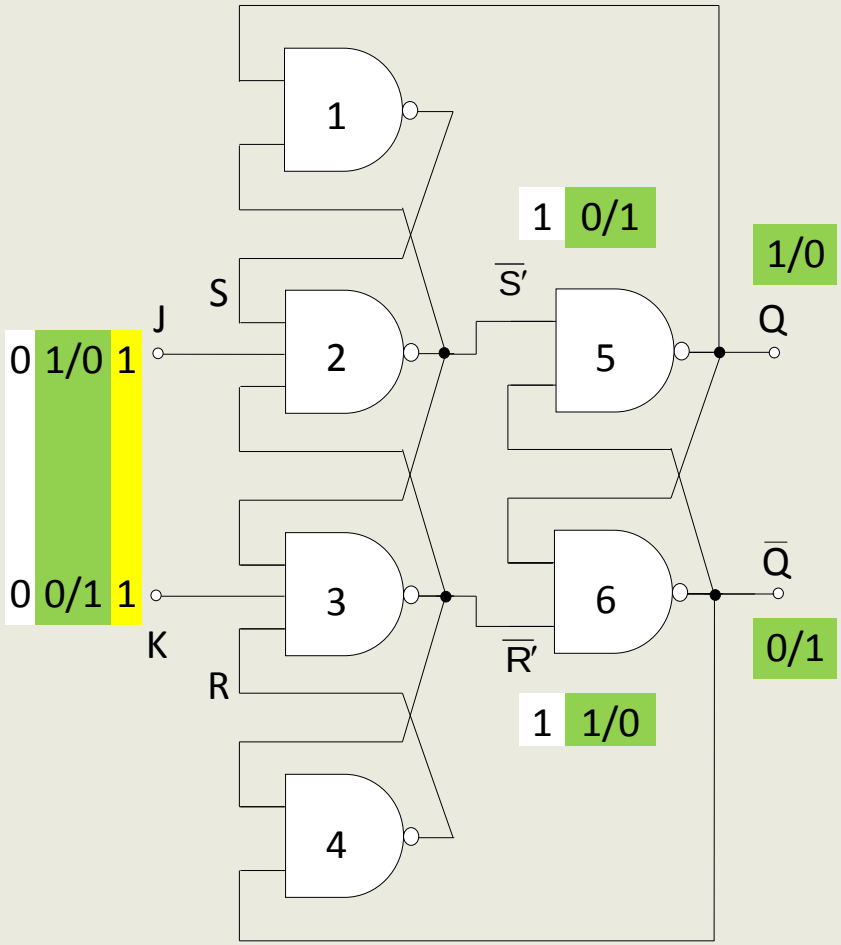
$$\overline{Q}^{t+1}_{SR} = R \vee \overline{S}\,\overline{Q}^t$$

$$Q^{t+1}_{JK} = J\overline{Q}^t \vee \overline{K}Q^t$$

$$\overline{Q}^{t+1}_{JK} = KQ^t \vee \overline{J}\,\overline{Q}^t$$

SR / Q^t	00	01	11	10
0	0	0	x	1
1	1	0	x	1

JK / Q^t	00	01	11	10
0	0	0	1	1
1	1	0	0	1



<u>J=0,K=0</u> → $\overline{S'}$=1,$\overline{R'}$=1 (*памет*);

<u>J=1,K=0</u> (**Q^t=1**;$\overline{S'}^t$=0)→S=1,($\overline{R'}^t$=1)→

$\overline{S'}^{t+1}$=0→**Q^{t+1} =1**;

(**Q^t=0**;$\overline{S'}^t$=1)→S=1,($\overline{R'}^{t+1}$=1, тъй като

в другото рамо K=1,R=1,$\overline{S'}^t$=1) $\overline{S'}^{t+1}$=0 →**Q^{t+1} =1**

<u>J=0,K=1</u> (**$\overline{Q}^t$=1**;$\overline{R'}^t$=0)→R=1, ($\overline{S'}^t$=1)→

$\overline{R'}^{t+1}$=0→ **$\overline{Q}^{t+1}$=1 (Q^{t+1}=0)**;

(**$\overline{Q}^t$=0**;$\overline{R'}^t$=1)→R=1,($\overline{R'}^{t+1}$=0), тъй като

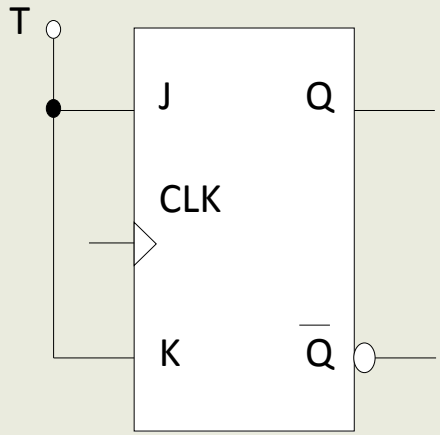
в другото рамо J=1,S=1,$\overline{R'}^t$=1)$\overline{R'}^{t+1}$=0→**Q^{t+1} =0**

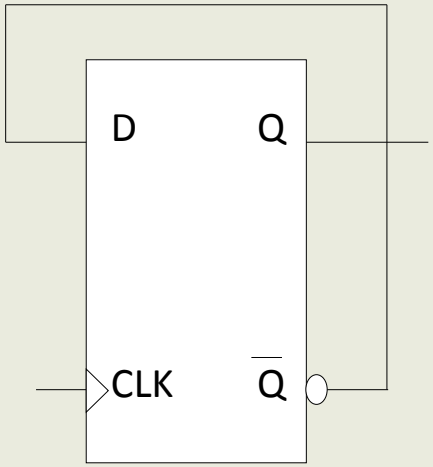
<u>J=1,K=1</u> (**Q^t=1**,$\overline{S'}^t$=0→**Q^{t+1}=0** (*смяна състояние*);

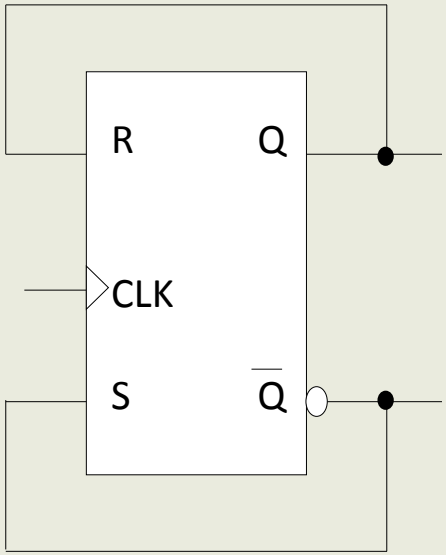
(**Q^t=0**,$\overline{S'}^t$=1→**Q^{t+1}=1** (*смяна състояние*)

T – тригери

Получаване от JK, D и RS тригери







$$Q^{t+1}{}_{JK} = J\overline{Q}^t \vee \overline{K}Q^t$$

$$Q^{t+1}{}_T = T\overline{Q}^t \vee \overline{T}Q^t$$

$$Q^{t+1}{}_D = D$$

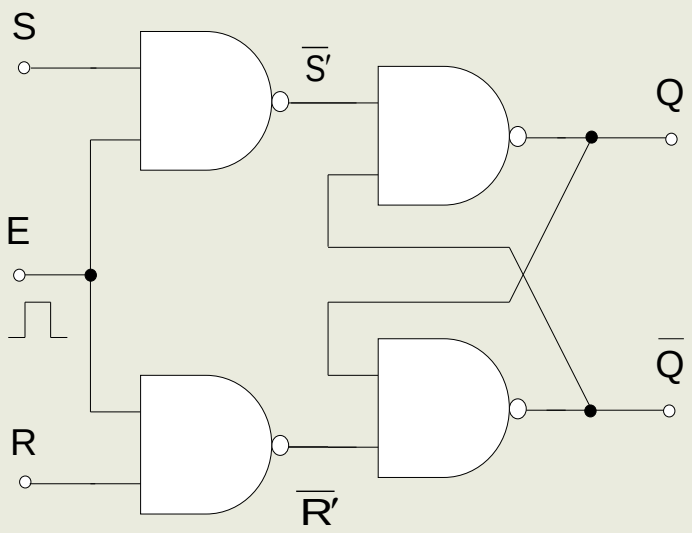
$$Q^{t+1}{}_T = T\overline{Q}^t \vee \overline{T}Q^t = 1.\overline{Q}^t (T = 1)$$

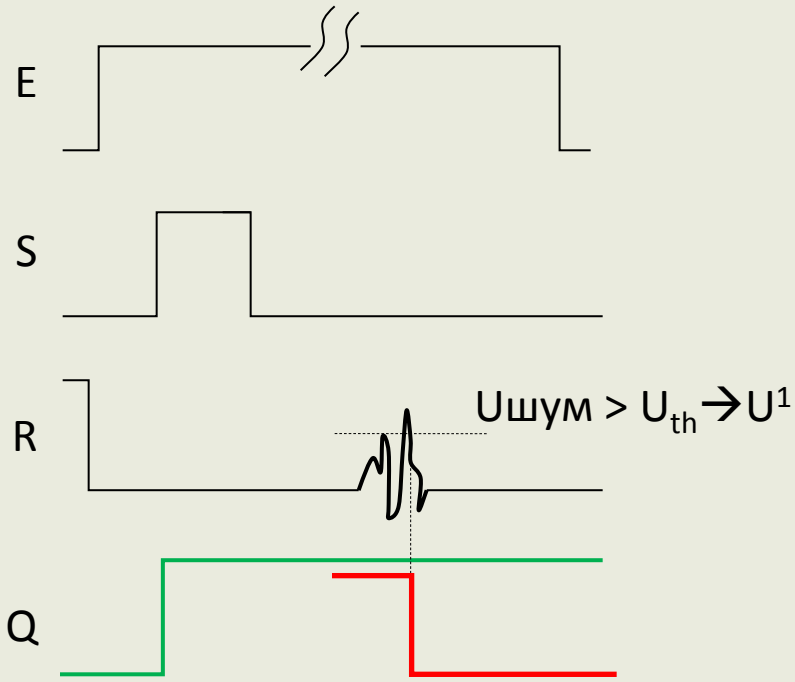
$$Q^{t+1}{}_{SR} = S \vee \overline{R}Q^t$$

$$Q^{t+1}{}_T = T\overline{Q}^t \vee \overline{T}Q^t (T = 1)$$

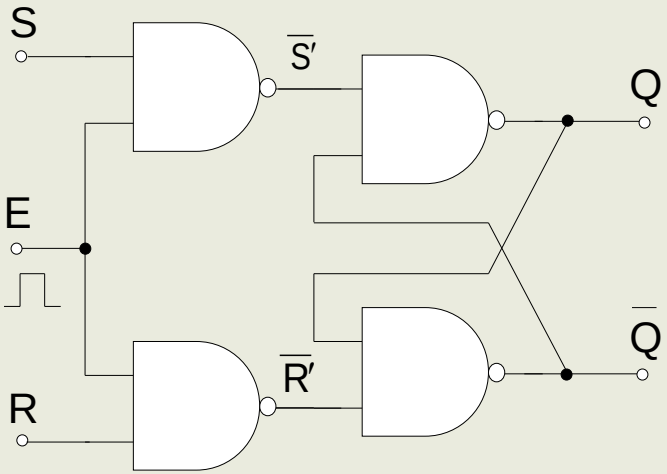
Синхронни по ниво тригери
(enabled / gated / с “логическо” разрешение)

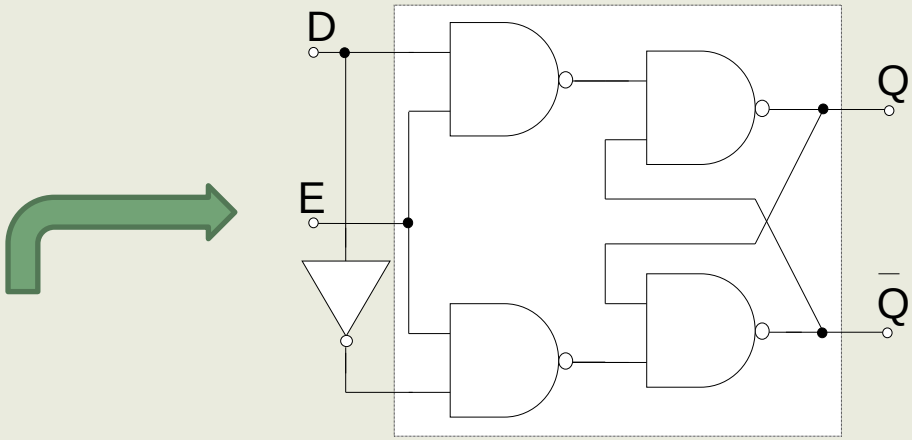
! Основен проблем при синхронните по ниво структури – липса на шумозащитеност на системно ниво. Възможност за промяна стойността на информационните входове <u>през цялото време</u>, през което E=high.

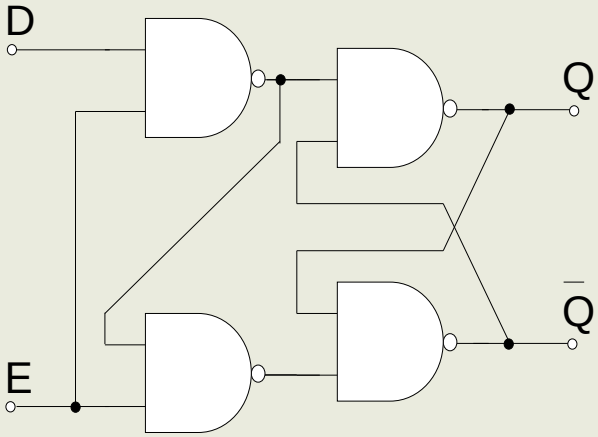




Синхронни по ниво тригери
(enabled / gated / с “логическо” разрешение)





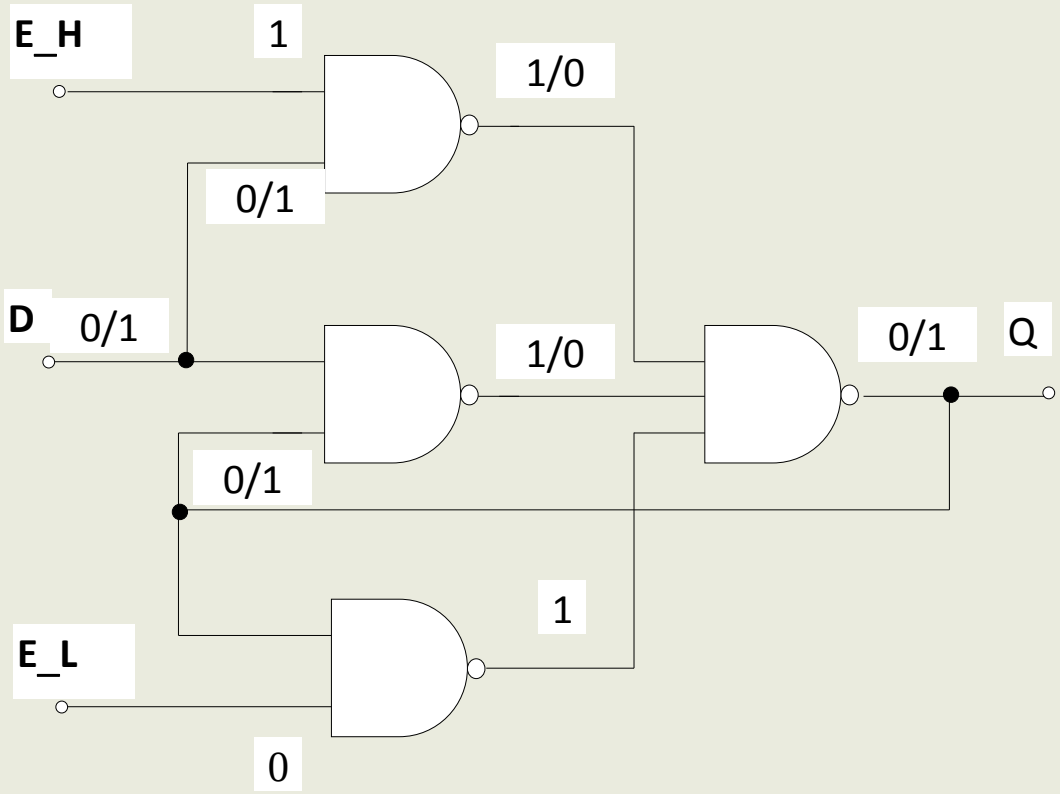


Допълнителни проблеми в горната схема:
- **голямо общо закъснение (3 гейта/ЛЕ);**
- **нееднакво закъснение при всички преходи (2 или 3 гейта);**
- **възможни са състезания на сигнали (hazards)**

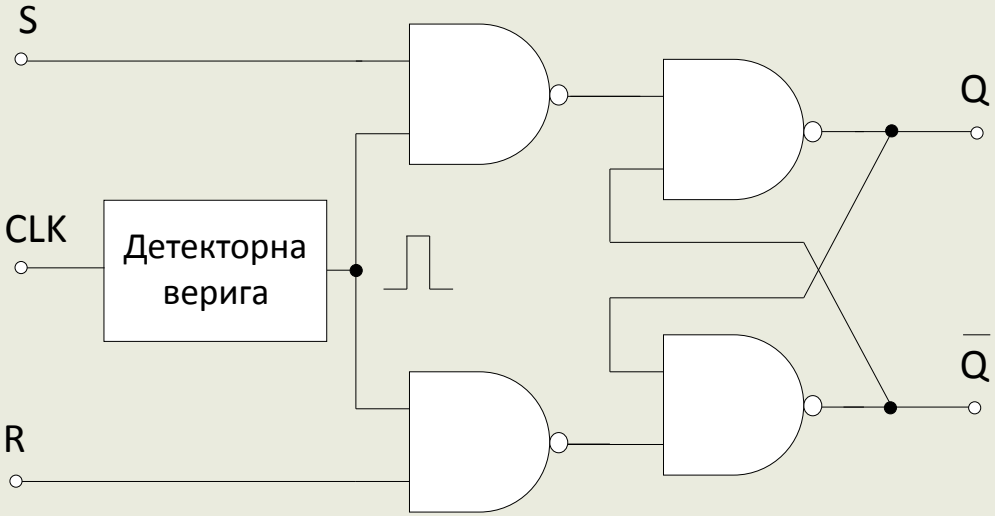
Синхронни по ниво тригери
(enabled / gated / с “логическо” разрешение)

Earle тригер

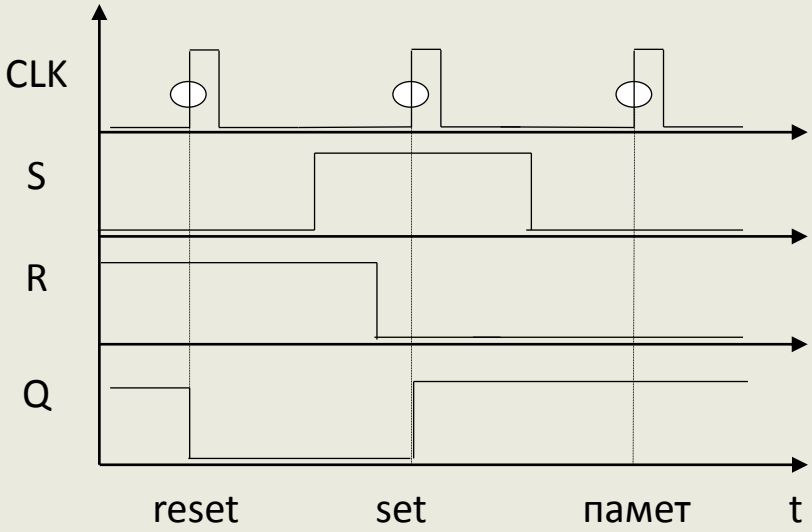
Схема с намалено закъснение (2 гейта) и липса на състезания на сигнали (hazard-free структура)



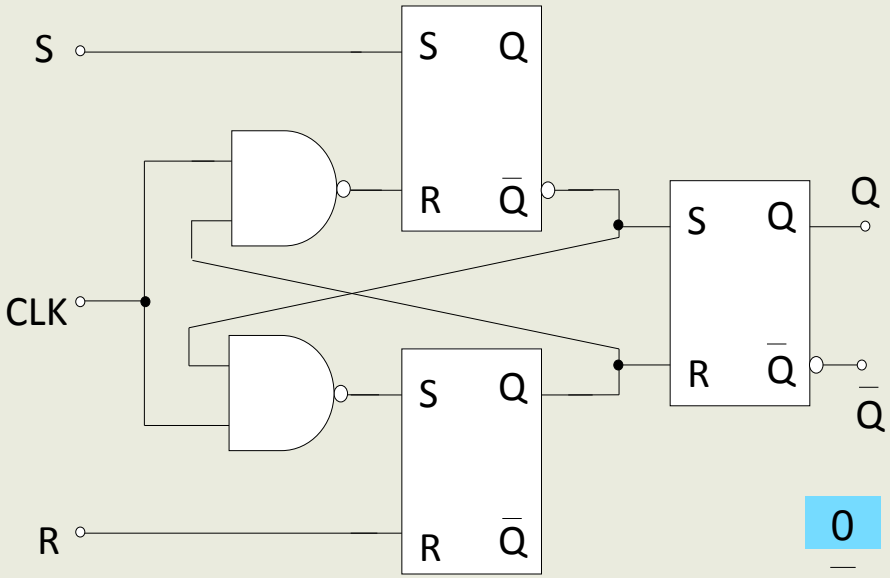
Синхронни тригери. Синхронни по фронт схеми

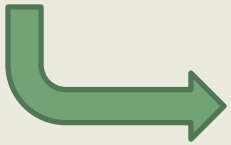


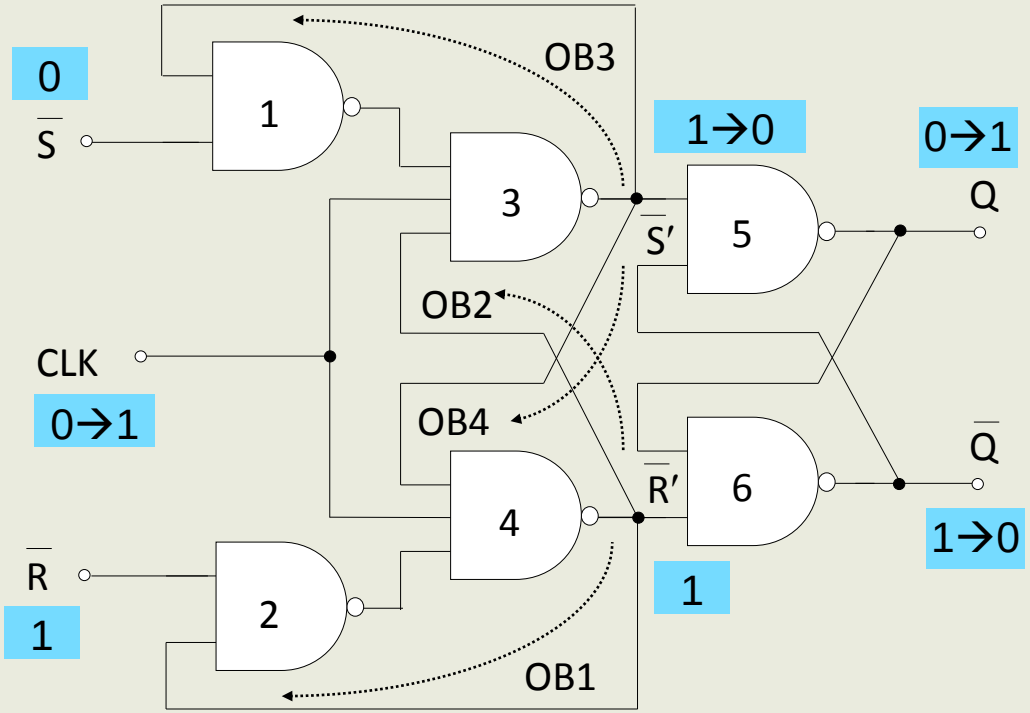
R	S	CLK	Q^{t+1}	действие
0	0	↑	Q^t	памет
0	1	↑	1	уст. в 1
1	0	↑	0	уст. в 0
1	1	↑	0	забранено



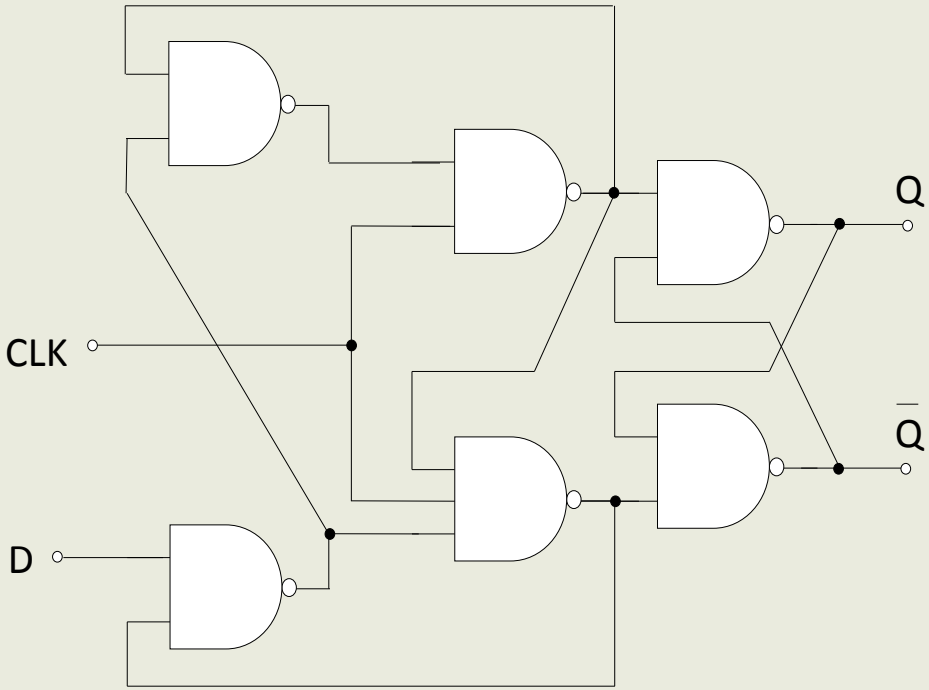
Синхронни по фронт тригери /RS тригер/

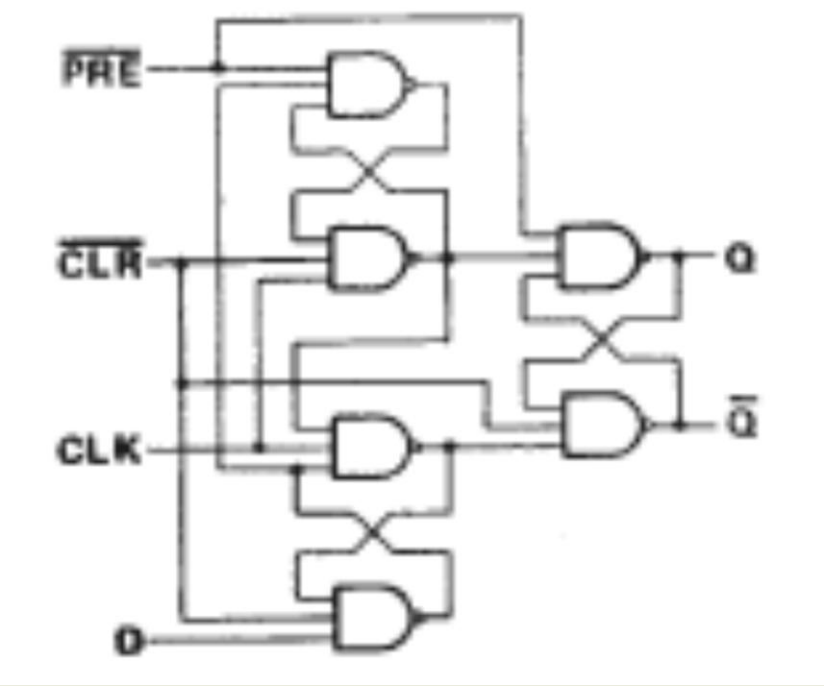






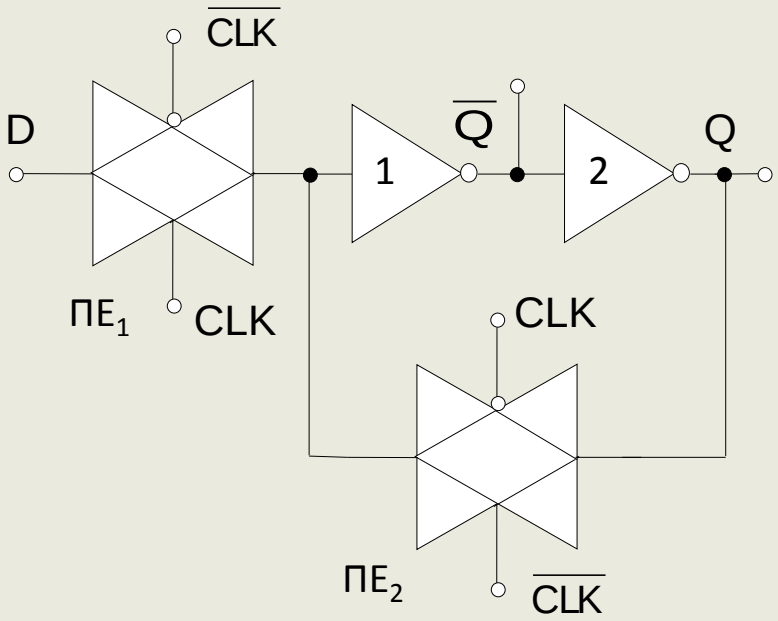
Синхронни по фронт тригери
/D тригер – схемно решение на Texas Instruments в ИС 7474/

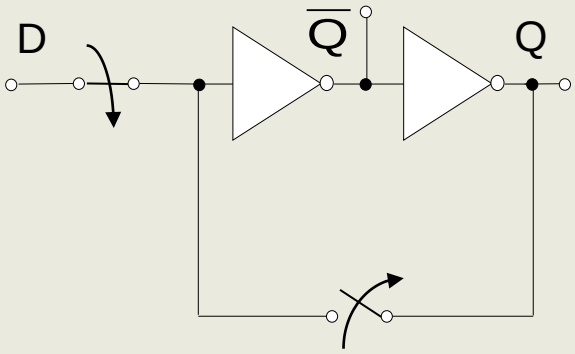


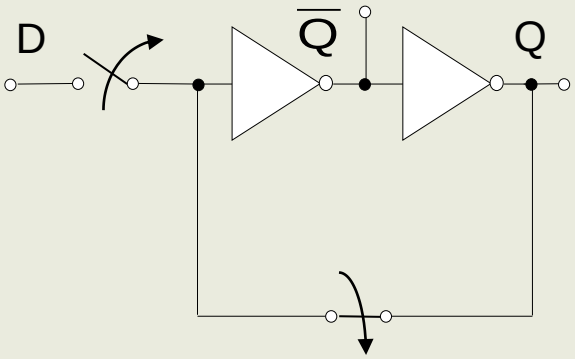


Схемно решение на **синхронен по преден фронт D-тригер** с асинхронни входове за нулиране и привеждане в единица (positive edge triggered flip-flop with preset and clear) на фирмата **Texas Instruments**

Синхронни по фронт тригери – D тригери с ПЕ (АК)

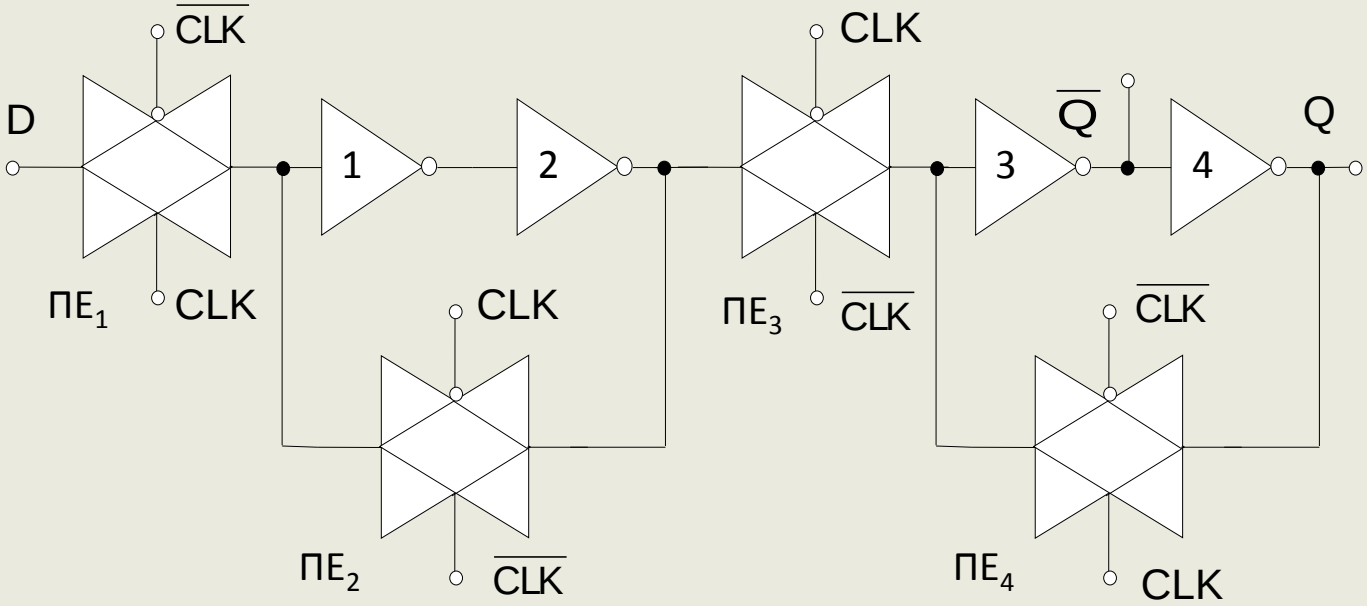


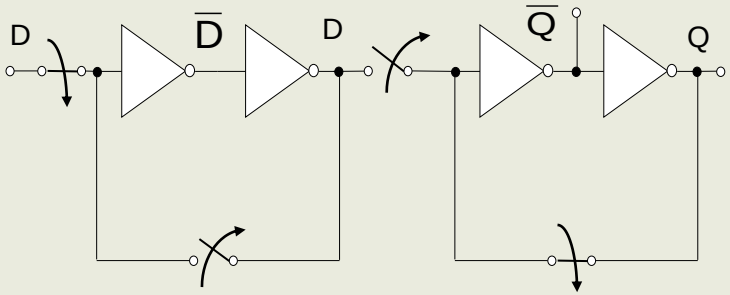


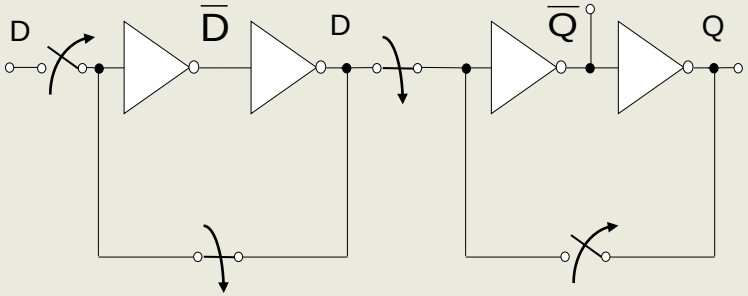


Синхронни по фронт тригери

MS D-тригер с ПЕ

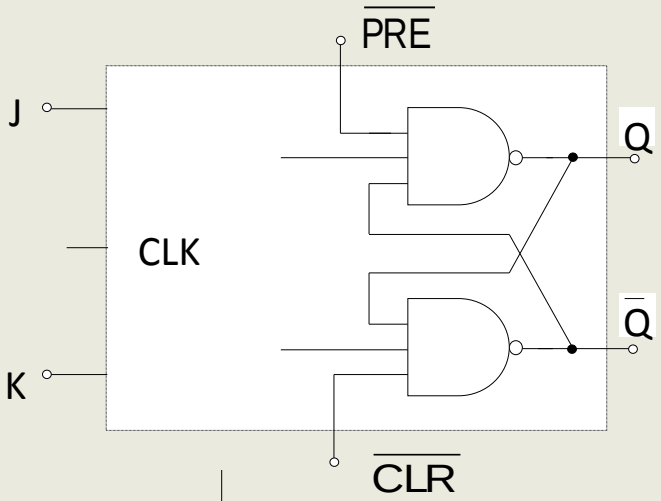


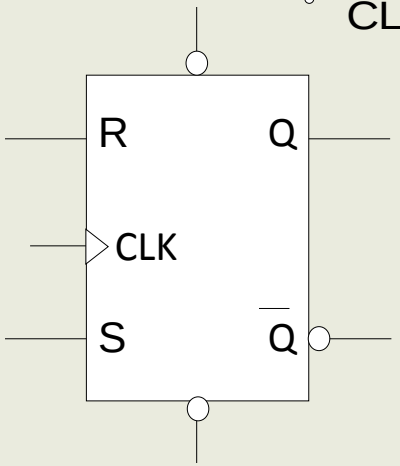


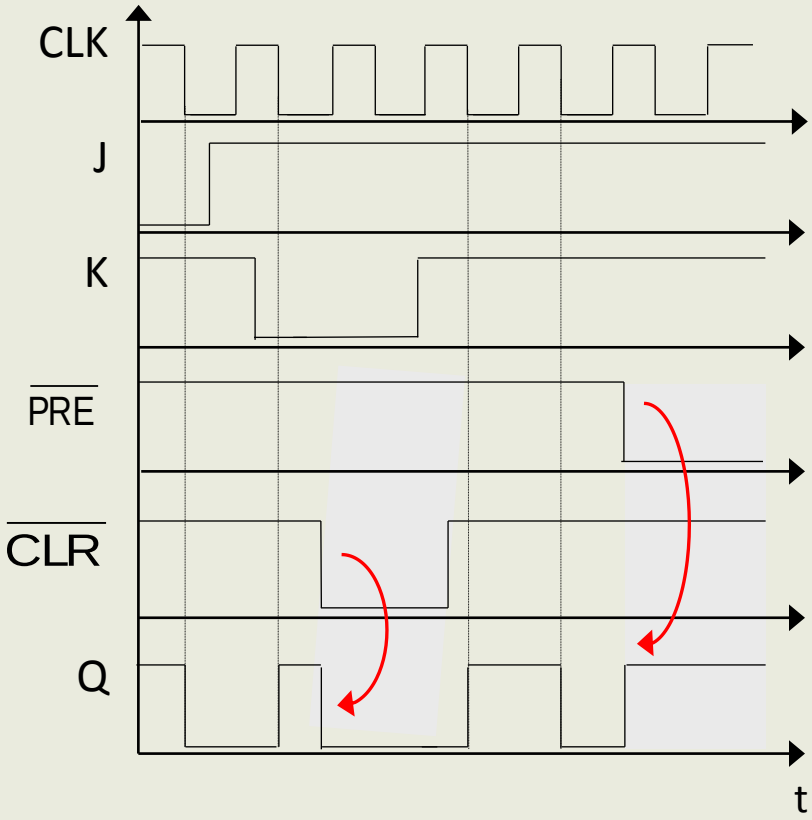


Асинхронно управление на синхронни тригерни структури

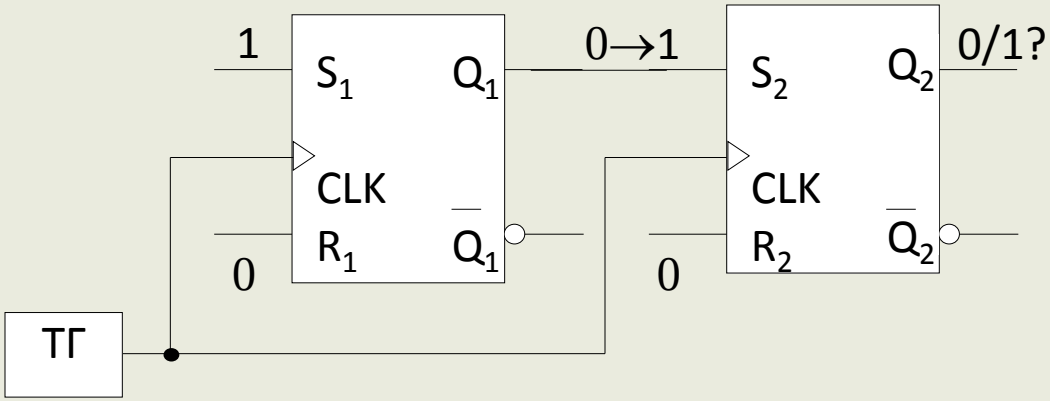
! Изискване (системно) – начално установяване на устройството (т.е. на всички тригери в него): нулиране, привеждане в конкретно състояние

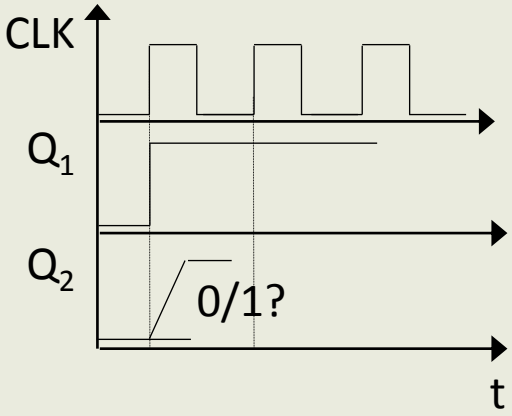




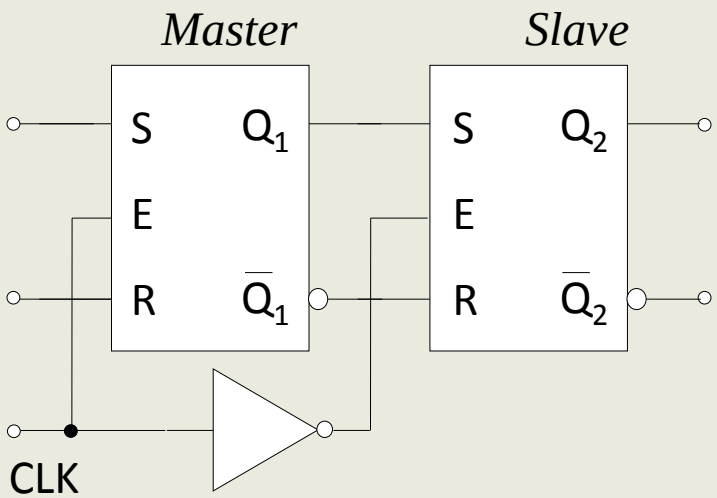


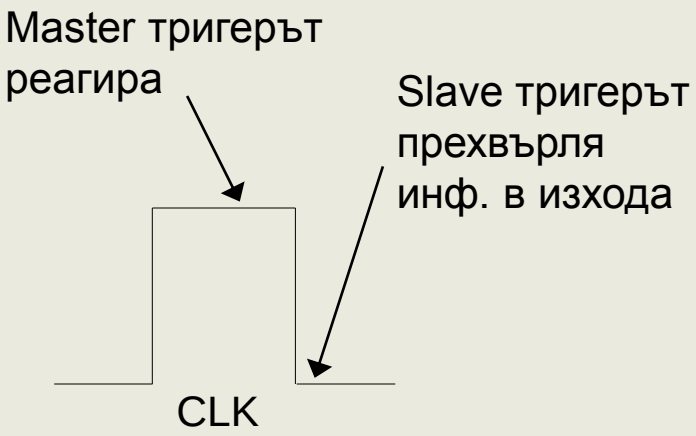
Състезания на сигнали в тригерни структури (пример)





Двустъпални тригери
Master-Slave структури, *pulse-triggered flip-flops*
RS MS тригер

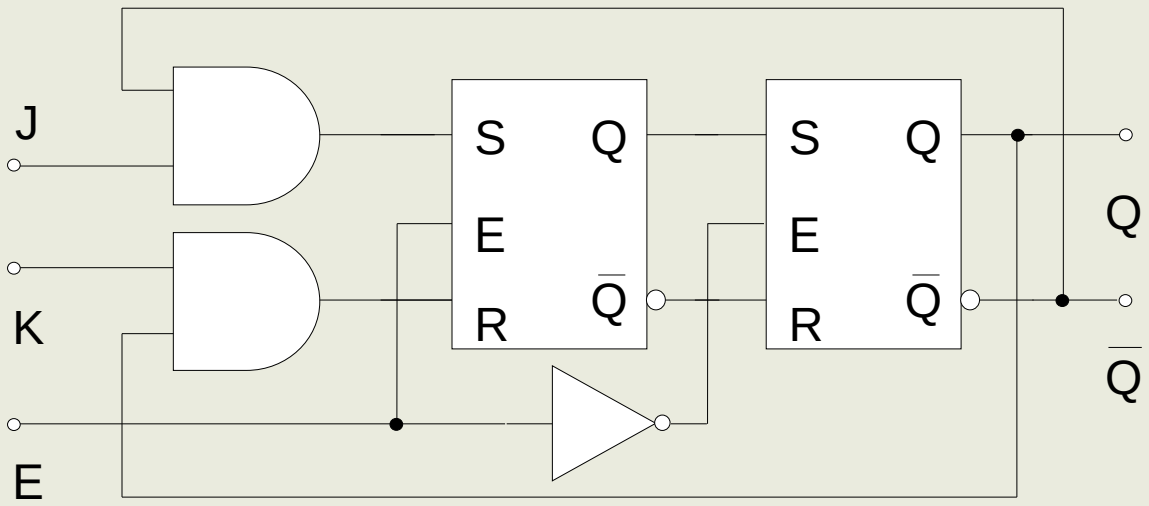


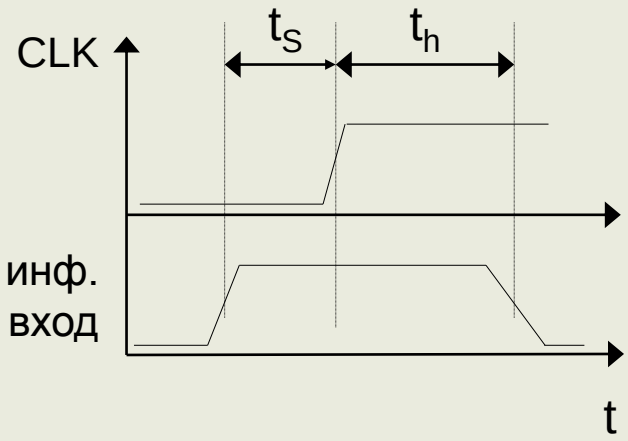


R	S	CLK	Q^{t+1}
0	0	⎍	Q^t
0	1	⎍	1
1	0	⎍	0
1	1	⎍	X

Двустъпални тригери

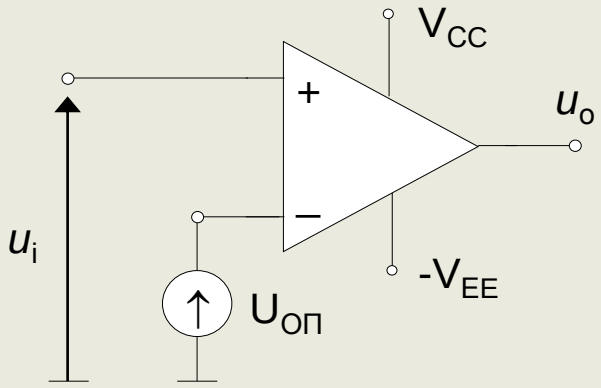
Примерна JK MS структура. Времеви параметри на тригери

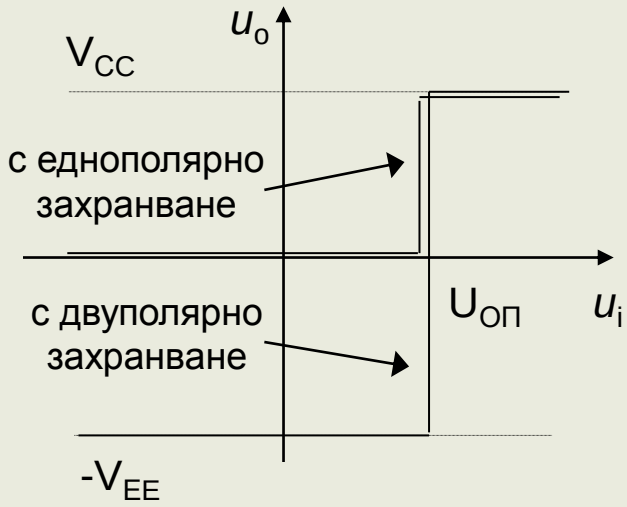


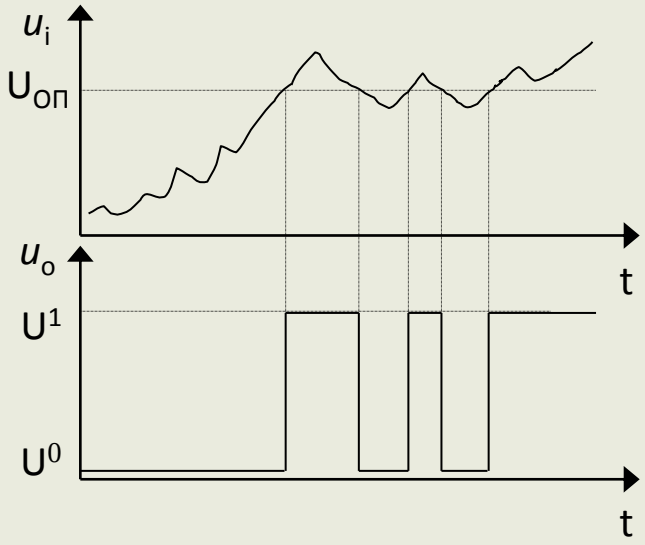


Несиметрични тригери

Принцип на схемите с хистерезис. Необходимост/функции

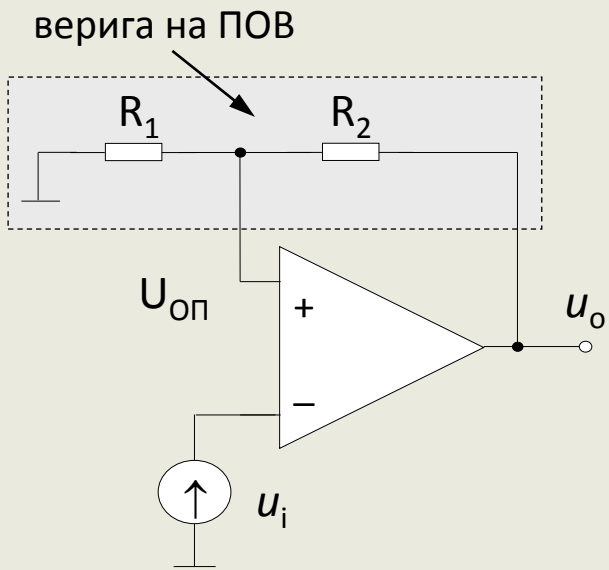






Несиметрични тригери

Принцип на схемите с хистерезис. Схема с ОУ



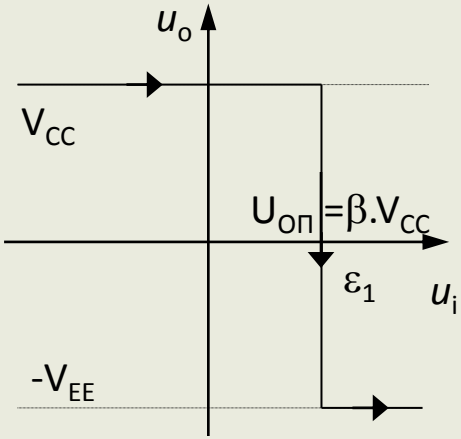
Нека $u_o = U^1$ и $u_i \uparrow$

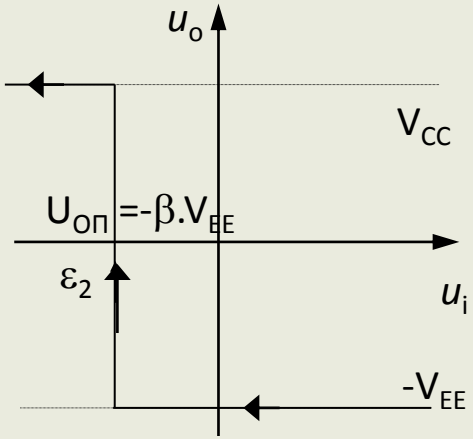
$$U_{ОП} = \beta . U^1 = \beta . V_{CC}$$

Нека $u_o = U^0$ и $u_i \downarrow$

$$U_{ОП} = \beta . U^0 = -\beta . V_{EE}$$

$$\beta = \frac{R_1}{R_1 + R_2} \qquad U_{ОП} = \beta . u_o$$

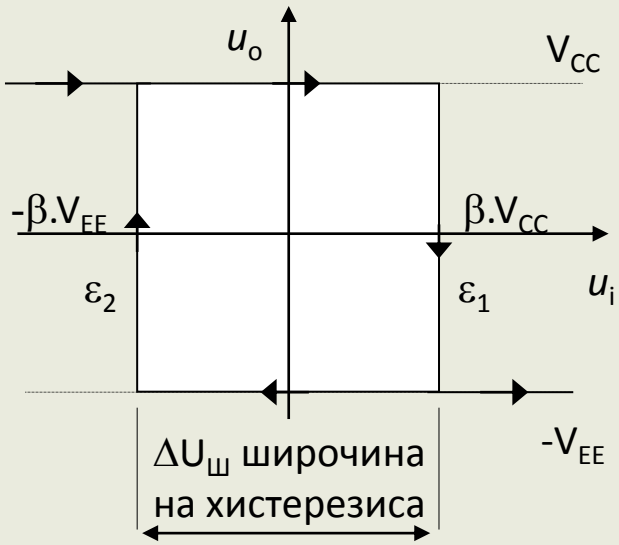


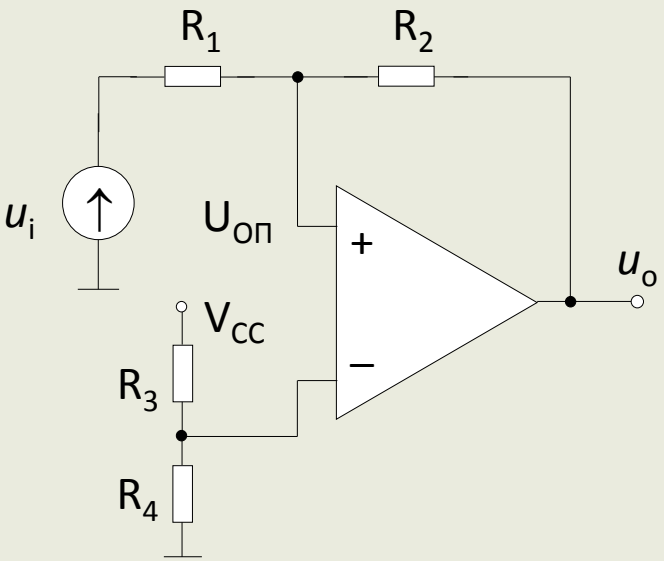


$$\varepsilon_1 = \frac{R_1}{R_1 + R_2} V_{CC}, \qquad \varepsilon_2 = -\frac{R_1}{R_1 + R_2} V_{EE}$$

Несиметрични тригери

ТШ с ОУ. Амплитуден хистерезис. Шумоустойчивост. Регулиране на праговете

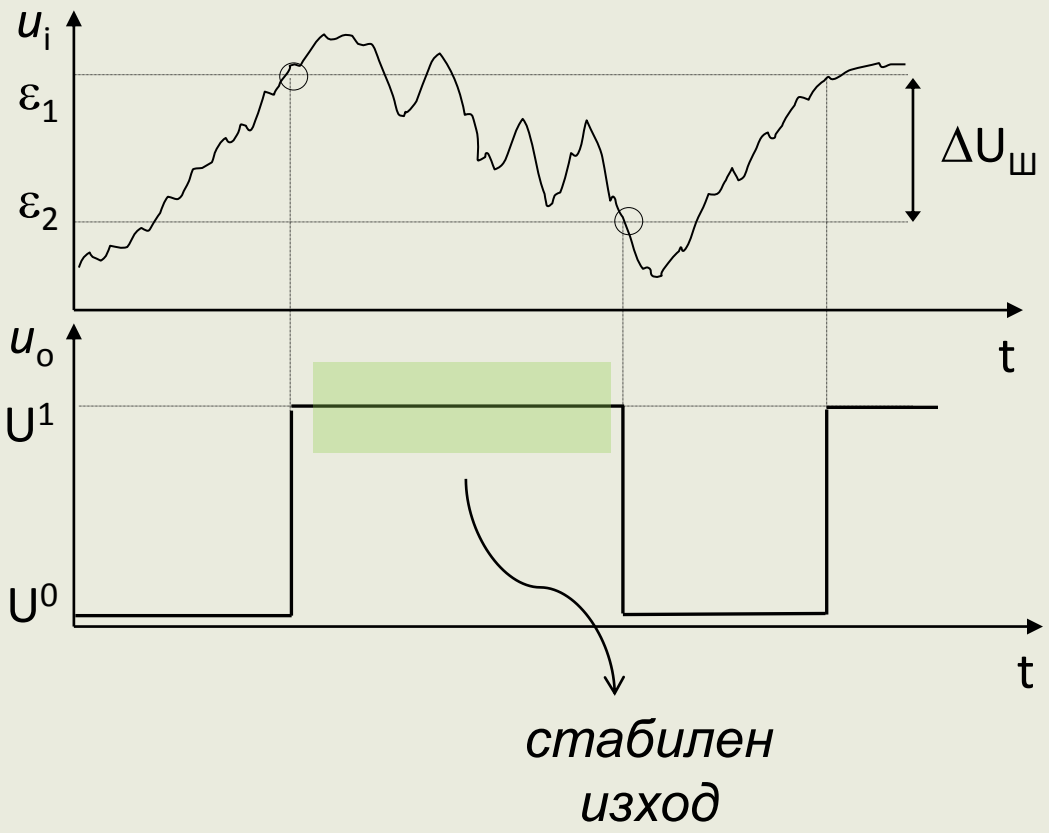




$$\Delta U_Ш = \beta.V_{CC} - (-\beta.V_{EE}) = \beta.(V_{CC} + V_{EE})$$

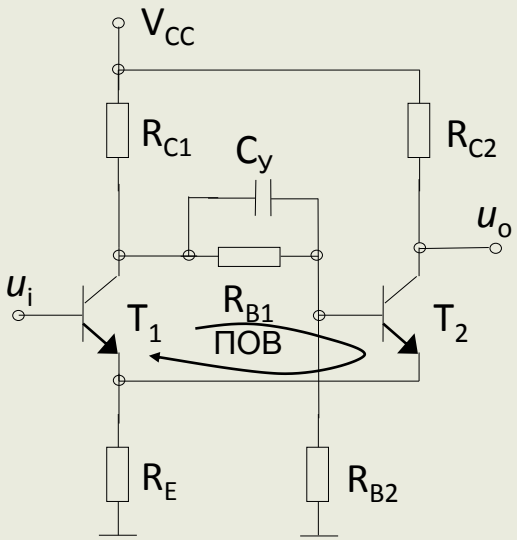
Несиметрични тригери

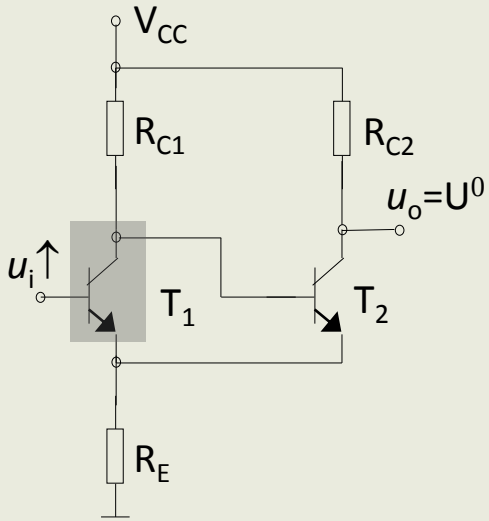
ТШ с ОУ. Амплитуден хистерезис. Шумоустойчивост

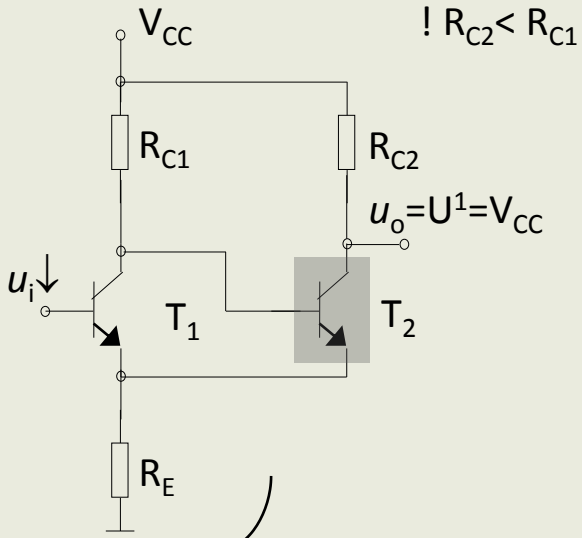


Несиметрични тригери

Транзисторен тригер е емитерна връзка







$$U^0 = U_{RE} + U_{CESAT}; \quad U_{RE} = \frac{R_E}{R_E + R_{C2}} V_{CC}$$

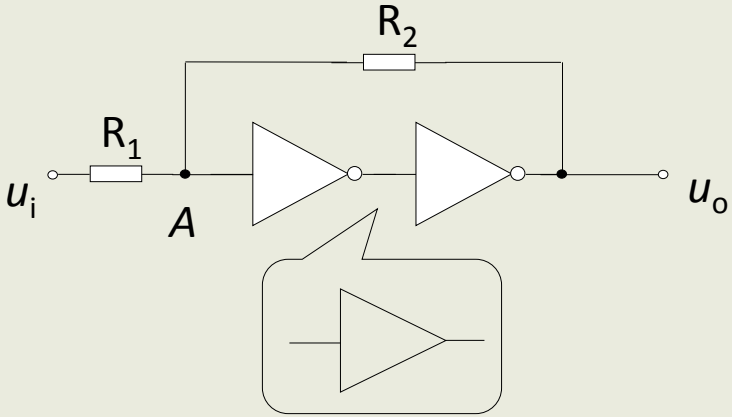
$$U^1 = V_{CC}$$

$$\varepsilon_1 = U_{RE} + U_{BE0} = \frac{R_E}{R_E + R_{C2}} V_{CC} + U_{BE0}$$

$$\varepsilon_2 = E_0 + \frac{R_E}{R_E + R_{C1}} (V_{CC} - U_{BE0})$$

Несиметрични тригери

ТШ с MOS/CMOS ЛЕ



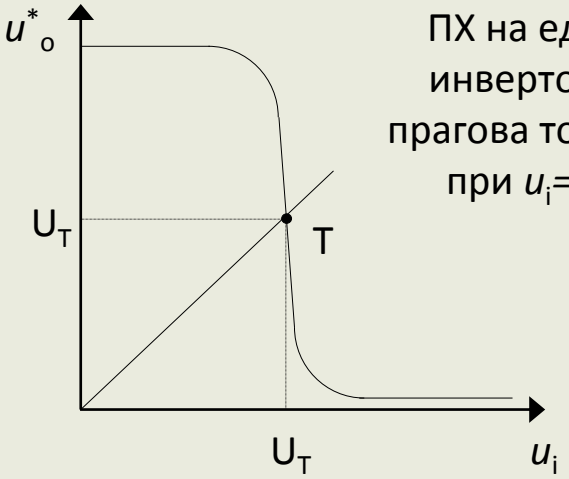
$$\beta . A_U > 1 \Rightarrow \frac{R_1 + R_2}{R_1} < A_U$$

$$U_T = u_i \frac{R_2}{R_1 + R_2} + u_0 \frac{R_1}{R_1 + R_2} = \frac{u_i R_2 + u_0 R_1}{R_1 + R_2}$$

$$\varepsilon_1 = U_T \frac{R_1 + R_2}{R_2} - U^0 \frac{R_1}{R_2}$$

$$\varepsilon_2 = U_T \frac{R_1 + R_2}{R_2} - U^1 \frac{R_1}{R_2} \ .$$

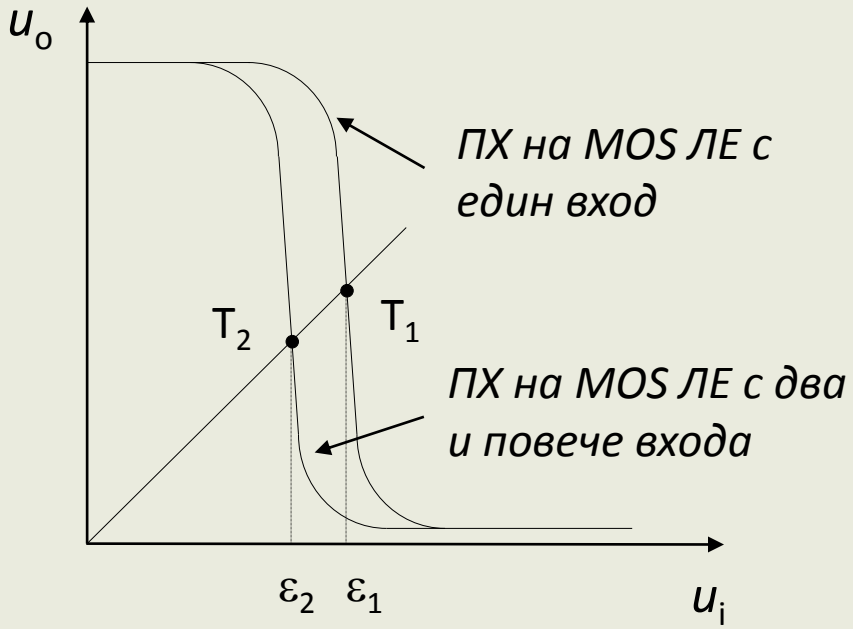
$$\Delta U = \varepsilon_1 - \varepsilon_2 = (U^1 - U^0).(R_1/R_2)$$

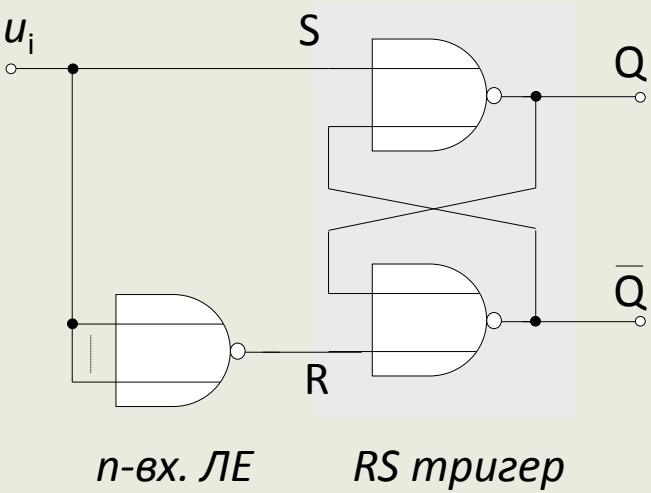


ПХ на един инвертор с прагова точка Т при $u_i = u_o$

Несиметрични тригери

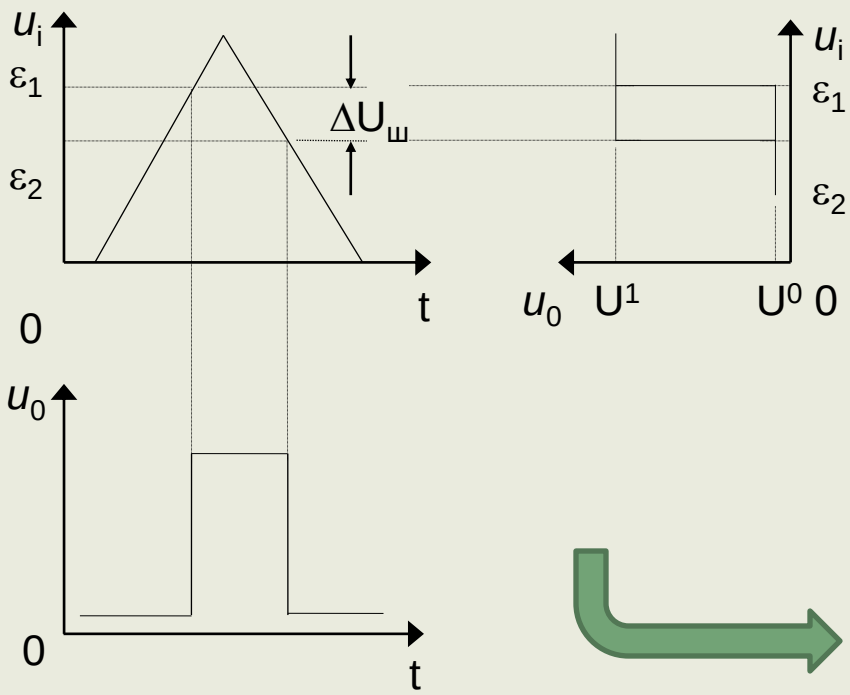
ТШ с RS тригер с MOS транзистори (примерно решение)

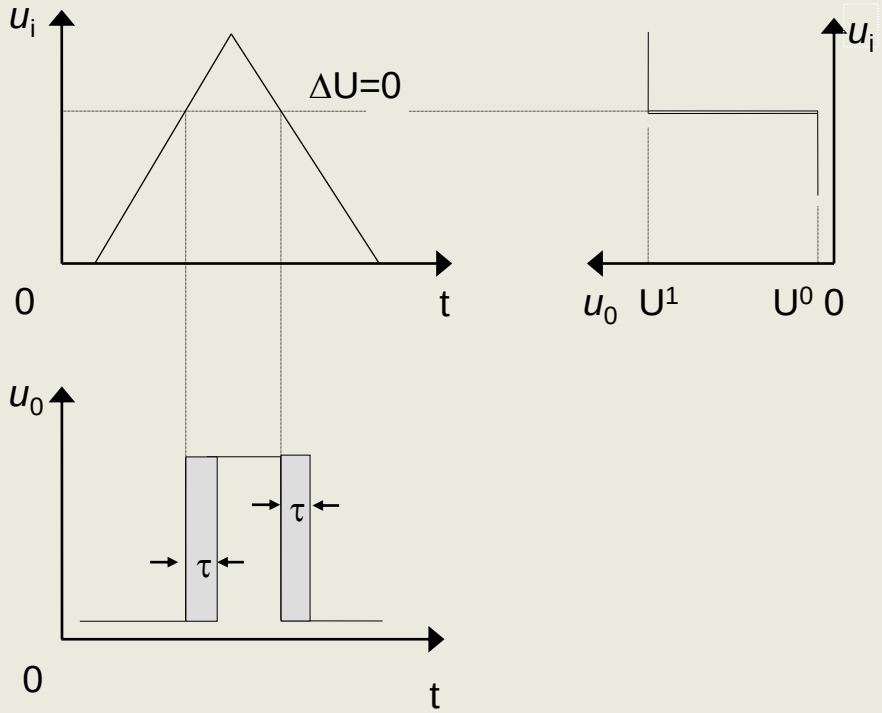




Несиметрични тригери

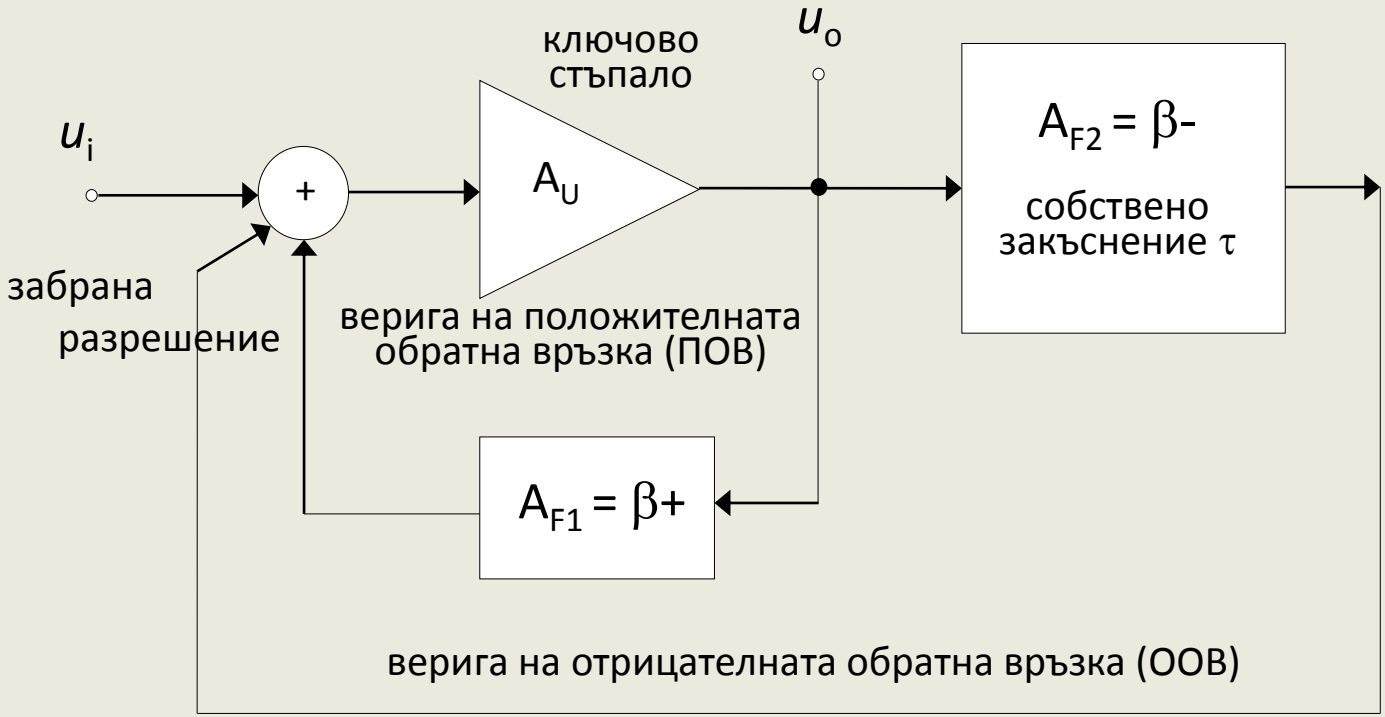
Схеми с “времеви” (time-domain) хистерезис. Принцип





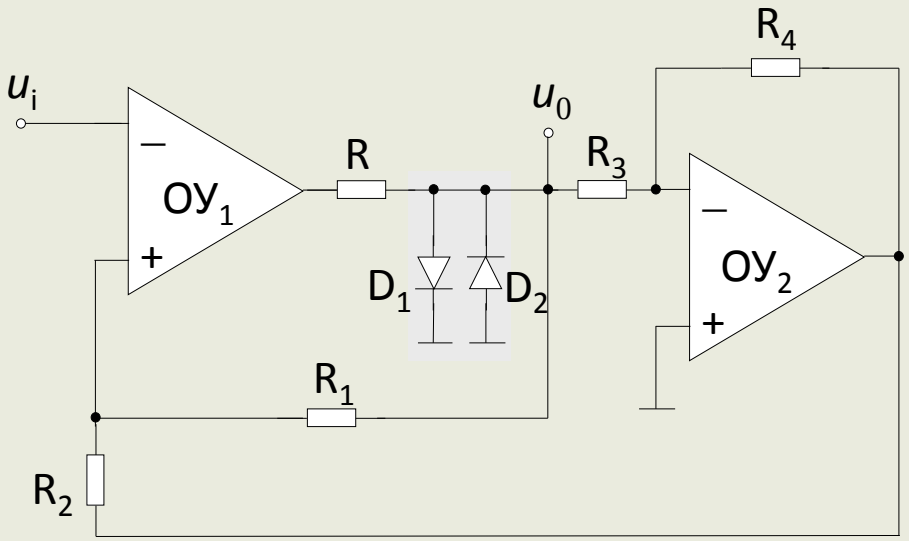
Несиметрични тригери

Схеми с “времеви” (time-domain) хистерезис. Обобщена схема

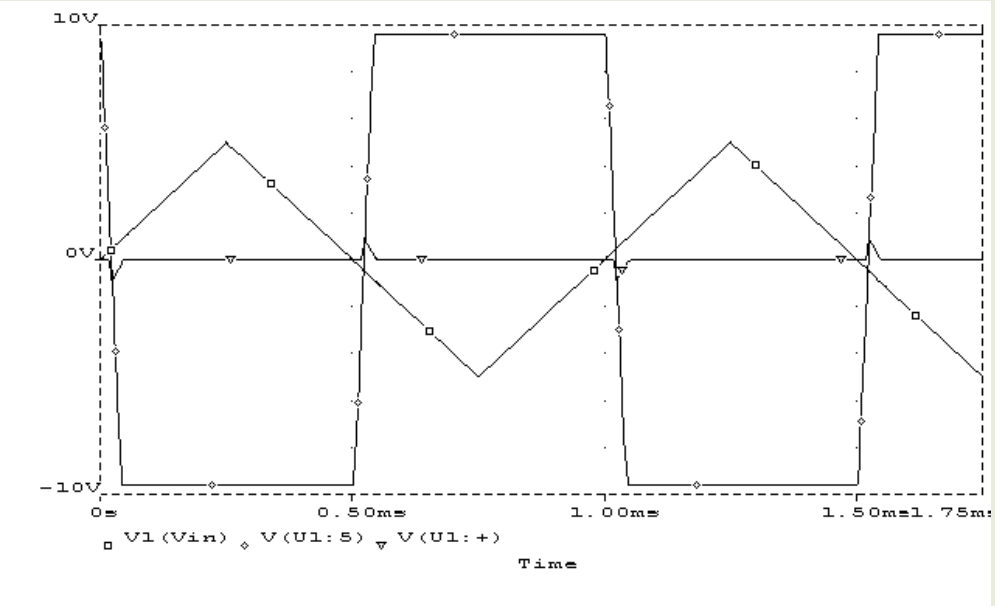


Несиметрични тригери

Схеми с “времеви” (time-domain) хистерезис. Схема с ОУ

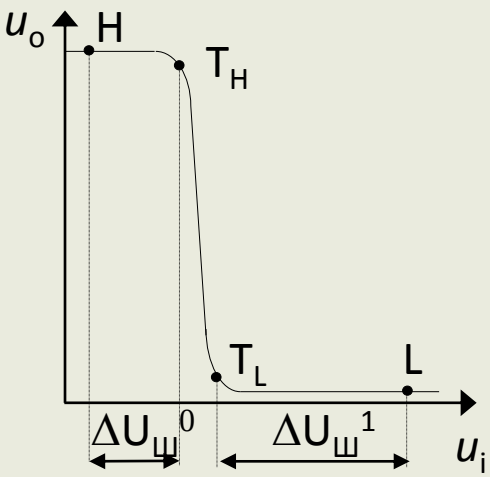


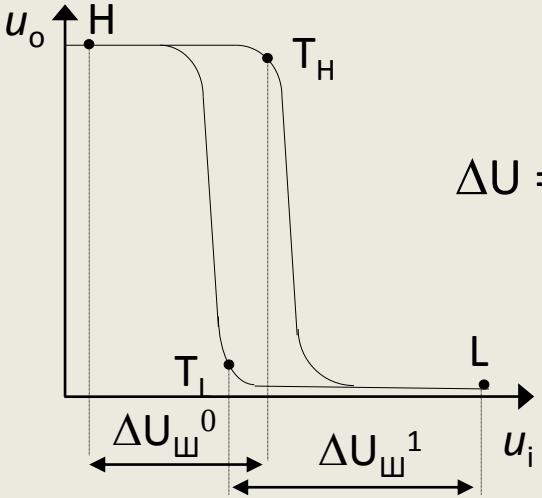
$R_1.R_4 = R_2.R_3$



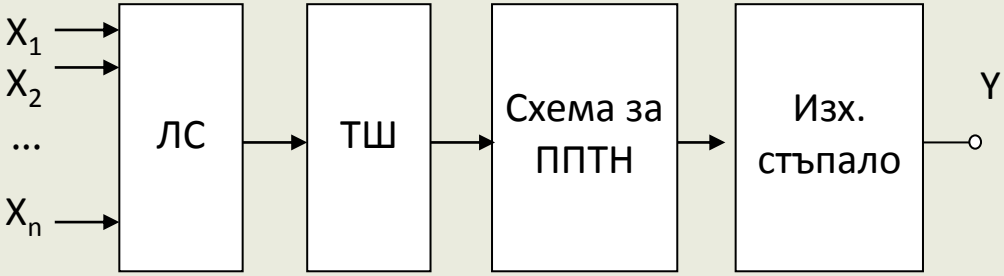
Логически схеми с хистерезис

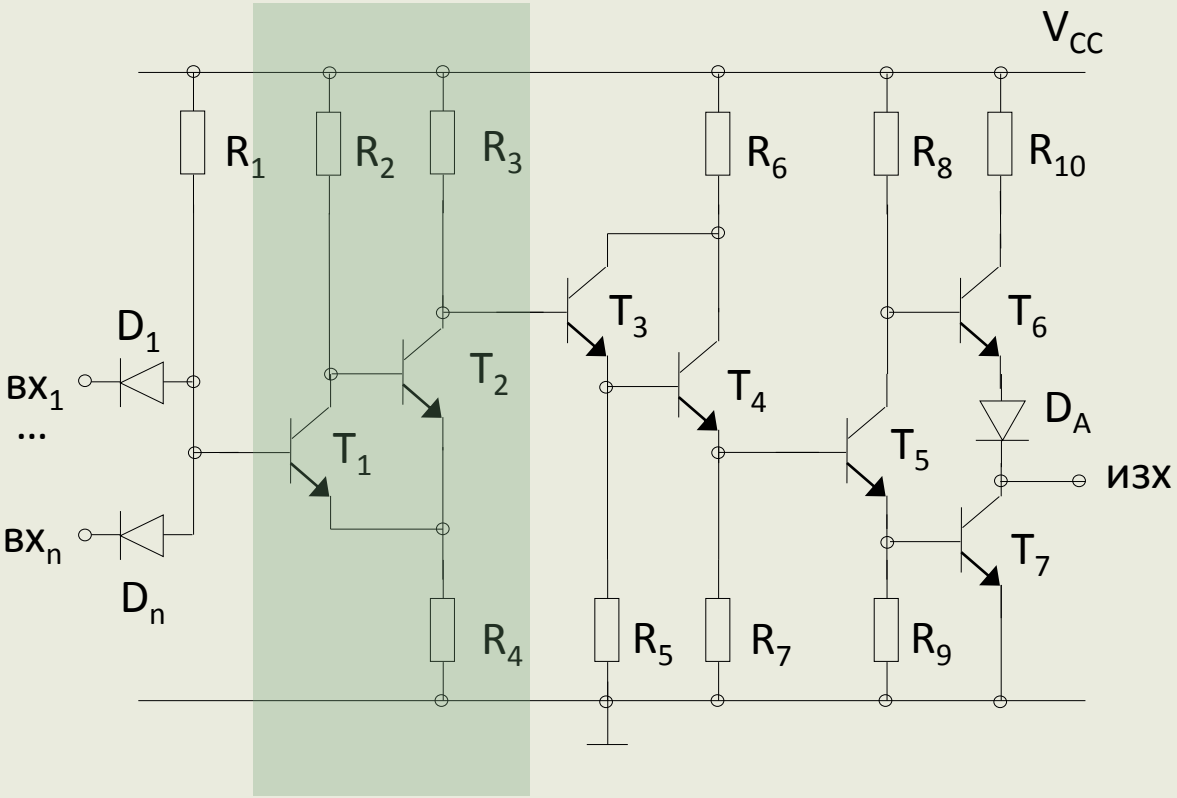
Предназначение, ПХ, обобщена структура на ЛС с хистерезис в TTL базис





$$\Delta U = |\Delta U_Ш^1 - \Delta U_Ш^0|$$



Логически схеми с хистерезис

Интегрална реализация в TTL-базис